

XPS-4341W-DXXG

(RoHS Compliant)

8.5 Gbps / 40 km / 100GHz DWDM XFP Single-Mode Optical Transceiver for 8G FC Applications

FEATURES

- Up to 8.5 Gb/s Bi-directional Data Link
- Complaint with XFP MSA
- Compliant with Fiber Channel FC-PI-4 800-SN-LL-L
- Compliant with 4G, 2G Fiber Channel
- SFF-8472 Digital Diagnostic Function
- **Maximum Link Length of 40 km**
- **Temperature-stabilized DWDM EML Transmitter**
- **100GHz ITU Grid, C Band**
- AC/AC Coupling according to MSA
- 2-Wire Interface for Integrated Digital Diagnostic Monitoring
- XFI Loopback Mode
- No reference Clock required
- Power Dissipation < 3.5 W
- +3.3 V & 5V Power Supply
- RoHS Compliant
- 0 to 70°C Operating
- Duplex LC Connector

APPLICATIONS

- Multi-rate 8x/4x/2x Fibre Channel

STANDARD

- Compliant with XFP MSA
- Compliant with 8GFC

LASER SAFETY

This single-mode transceiver is a Class 1 laser product. It complies with IEC-60825 and FDA 21 CFR 1040.10 and 1040.11. The transceiver must be operated within the specified temperature and voltage limits. The optical ports of the module shall be terminated with an optical connector or with a dust plug.

DESCRIPTION

XPS-4341W-DXXG series multi-rate 8G XFP transceivers are designed for serial optical data communications such as 8G Fibre Channel. It supports the 8.5Gbps transmission on 9/125 μm SMF.

This module is designed for single mode fiber and operates at a nominal wavelength of 100GHz ITU Grid, C Band DWDM wavelength. The transmitter section consists of a temperature-stabilized DWDM electrical-modulated laser (EML), driver and signal conditioner. The receiver section incorporates a PIN photodiode integrated with a trans-impedance preamplifier (TIA) and signal conditioner.

The module is with the XFP 30-pin connector to allow hot plug capability. Integrated Tx and Rx signal conditioners provide high jitter-tolerance for full XFI compliance and no external reference clock required. The internally ac coupled high speed serial I/O simplifies interfacing to external circuitry. Dual 5V and 3.3V power supply are used. The optical output can be disabled by LVTTTL logic high-level input of TX_DIS. Loss of signal (RX_LOS) output is provided to indicate the loss of an input optical signal of receiver.

A serial EEPROM in the transceiver allows the user to access transceiver digital diagnostic monitoring and configuration data via the 2-wire XFP Management Interface. This interface uses a single address, A0h, with a memory map divided into a lower and upper area. Basic digital diagnostic data is held in the lower area while specific data is held in a series of tables in the high memory area.

ORDER INFORMATION

P/No.	Bit Rate (Gb/s)	FC-PI	Distance (km)	Spacing (GHz)	Wavelength (nm)	Package	Case Temp (°C)	RoHS Compliant
XPS-4341W-DXXG	8 / 4 / 2	FC-PI-4	40	100	DWDM*	XFP with DMI	0 to 70	Yes

*XX: 100GHz ITU Grid wavelength (Please see below)

Channel #	Product code	Frequency (THz)	Center Wavelength (nm)	Label
19	XPS-4341W-D19G	191.9	1562.23	D19
20	XPS-4341W-D20G	192.0	1561.42	D20
21	XPS-4341W-D21G	192.1	1560.61	D21
22	XPS-4341W-D22G	192.2	1559.79	D22
23	XPS-4341W-D23G	192.3	1558.98	D23
24	XPS-4341W-D24G	192.4	1558.17	D24
25	XPS-4341W-D25G	192.5	1557.36	D25
26	XPS-4341W-D26G	192.6	1556.55	D26
27	XPS-4341W-D27G	192.7	1555.75	D27
28	XPS-4341W-D28G	192.8	1554.94	D28
29	XPS-4341W-D29G	192.9	1554.13	D29
30	XPS-4341W-D30G	193.0	1553.33	D30
31	XPS-4341W-D31G	193.1	1552.52	D31
32	XPS-4341W-D32G	193.2	1551.72	D32
33	XPS-4341W-D33G	193.3	1550.92	D33
34	XPS-4341W-D34G	193.4	1550.12	D34
35	XPS-4341W-D35G	193.5	1549.32	D35
36	XPS-4341W-D36G	193.6	1548.51	D36
37	XPS-4341W-D37G	193.7	1547.72	D37
38	XPS-4341W-D38G	193.8	1546.92	D38
39	XPS-4341W-D39G	193.9	1546.12	D39
40	XPS-4341W-D40G	194.0	1545.32	D40
41	XPS-4341W-D41G	194.1	1544.53	D41
42	XPS-4341W-D42G	194.2	1543.73	D42
43	XPS-4341W-D43G	194.3	1542.94	D43
44	XPS-4341W-D44G	194.4	1542.14	D44
45	XPS-4341W-D45G	194.5	1541.35	D45
46	XPS-4341W-D46G	194.6	1540.56	D46
47	XPS-4341W-D47G	194.7	1539.77	D47
48	XPS-4341W-D48G	194.8	1538.98	D48
49	XPS-4341W-D49G	194.9	1538.19	D49
50	XPS-4341W-D50G	195.0	1537.40	D50
51	XPS-4341W-D51G	195.1	1536.61	D51
52	XPS-4341W-D52G	195.2	1535.82	D52
53	XPS-4341W-D53G	195.3	1535.04	D53
54	XPS-4341W-D54G	195.4	1534.25	D54
55	XPS-4341W-D55G	195.5	1533.47	D55
56	XPS-4341W-D56G	195.6	1532.68	D56
57	XPS-4341W-D57G	195.7	1531.90	D57
58	XPS-4341W-D58G	195.8	1531.12	D58
59	XPS-4341W-D59G	195.9	1530.33	D59
60	XPS-4341W-D60G	196.0	1529.55	D60
61	XPS-4341W-D61G	196.1	1528.77	D61

Absolute Maximum Ratings					
Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	Tstg	-40	85	°C	
Operating Case Temperature	Topr	0	70	°C	
Relative Humidity	RH	0	85	%	Non condensing
Power Supply Voltage (5V)	Vcc5	-0.5	6.0	V	
Power Supply Voltage (3.3V)	Vcc3	-0.5	3.6	V	
Receiver Input Optical Power	Mip		4	dBm	Received average power

Recommended Operating Conditions					
Parameter	Symbol	Min	Typ	Max	Units / Notes
Power Supply Voltage (5V)	Vcc5	4.75	5	5.25	V
Power Supply Voltage (3.3V)	Vcc3	3.13	3.3	3.47	V
Power Supply Current (@5V)	Icc5			500	mA / 1
Power Supply Current (@3.3V)	Icc3			750	mA / 1
Power Dissipation	Pd			3.5	W
Operating Case Temperature	Topr	0		70	°C
Data Rate			8.5		Gb/s

1. Including in rush current. Maximum module current ramp rate is 100 mA/μs.

Transmitter Optical Specifications (Topr= 0 to 70°C, Vcc5=5V±5%, Vcc3 = 3.3V ±5%)						
Parameter	Symbol	Min	Typ	Max	Units	Notes
Average Launch Power	P _{O, Avg}	-2		+2	dBm	2
Extinction Ratio	ER	8.2			dB	
Center Wavelength Spacing			100		GHz	3
Transmitter Center Wavelength -- over life time	λ _c	X-100	X	X+100	pm	4
Output Spectrum Width	σ _λ			1	nm	-20 dB width
Side Mode Suppression Ratio	SMSR	30			dB	
Relative Intensity Noise	RIN			-130	dB/Hz	
Average Launch Power of OFF Transmitter				-30	dBm	

2. Output power is power coupled into a 9/125 μm single-mode fiber.

3. Corresponds to approximately 0.8 nm.

4. X = specified ITU Grid wavelength. Wavelength stability is achieved within 60 seconds of power up.

Receiver Optical Specifications (Topr= 0 to 70°C, Vcc5=5V±5%, Vcc3 = 3.3V ±5%)						
Parameter	Symbol	Min	Typ	Max	Units	Notes
Sensitivity	Sen1			-16	dBm	5
Receiver Overload	P _{MAX}	-1	---		dBm	
Dispersion Penalty	Dp			2	dB	5
LOS -- Deasserted	LOS _D	---	---	-20	dBm	Transition: low to high
LOS -- Asserted	LOS _A	-28	---	---	dBm	Transition: high to low
LOS -- Hysteresis		0.5	---		dB	
Wavelength of Operation	λ _c	1260		1620	nm	

5. Measured with worst ER; BER < 10⁻¹² and PRBS 2⁷-1.

Electrical Characteristics						
Parameter	Symbol	Min	Typ	Max	Units	Notes
High-Speed Signal (CML) Interface Specification						
Input Data Rate			8.5		Gb/s	
TX Clock Tolerance				±100	ppm	6
Differential Input Impedance	R _{in}		100		Ω	
Differential Data Input Amplitude		120		820	mV _{pp}	7, Internally AC coupled
Output Data Rate			8.5		Gb/s	
RX Clock Tolerance				±100	ppm	6
Differential Output Impedance	R _{out}		100		Ω	
Differential Data Output Amplitude		340		850	mV _{pp}	7, Internally AC coupled
Low-Speed Signal (LVTTTL) Interface Specification						
Input High Voltage		2.0		V _{cc}	V	
Input Low Voltage		GND		0.8	V	
Output High Voltage		2.4		V _{cc}	V	
Output Low Voltage		GND		0.5	V	
Reference Clock (LVPECL) Interface Specification						
No reference clock						

6. Clock tolerance for 8.5 Gb/s, 4.25 Gb/s, 2.12 Gb/s.

7. The differential input and output amplitudes are per XFP MSA mask at points B' and C'.

Transceiver Timing Characteristics						
Parameter	Symbol	Min	Typ	Max	Units	Notes
TX_DIS Assert Time	t _{off}			10	μs	
TX_DIS Negate Time	t _{on}			2	ms	
Time to Initialize	t _{init}			300	ms	
Interrupt Assert Delay	interrupt _{on}			200	ms	
Interrupt Negate Delay	interrupt _{off}			500	μs	
P_Down/PST Assert Delay	P_Down/RST _{on}			100	μs	
P_Down Negate Delay	P_Down/RST _{off}			300	ms	
Mod_NR Assert Delay	Mod_nr _{on}			1	ms	
Mod_NR Negate Delay	Mod_nr _{off}			1	ms	
Mod_Desel Assert Time	T_Mod_Desel			2	ms	
Mod_Desel De-Assert Time	T_Mod_Sel			2	ms	
P_Down Reset Time	T _{reset}	10			μs	
RX_LOS Assert Delay	T _{Los_{on}}			100	μs	
RX_LOS Negate Delay	T _{Los_{off}}			100	μs	
Serial ID Clock Rate	f _{SCL}	0		400	kHz	

MANAGEMENT INTERFACE

The structure of the memory map is shown in Figure 1, which is accessible over a 2-wire serial interface at the 8-bit address 1010000X (A0h). The normal 256 byte I2C address space is divided into low and upper blocks of 128 Bytes. The lower block of 128 Bytes is always directly available and is used for the diagnostics and control function. Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. Thus, there is a total available address space of 128*256 = 32 Kbytes in this upper memory space. The contents of Table 01h are listed in Table 1 below. Please refer SFF INF-8077i (Revision 4.5) for detailed information.

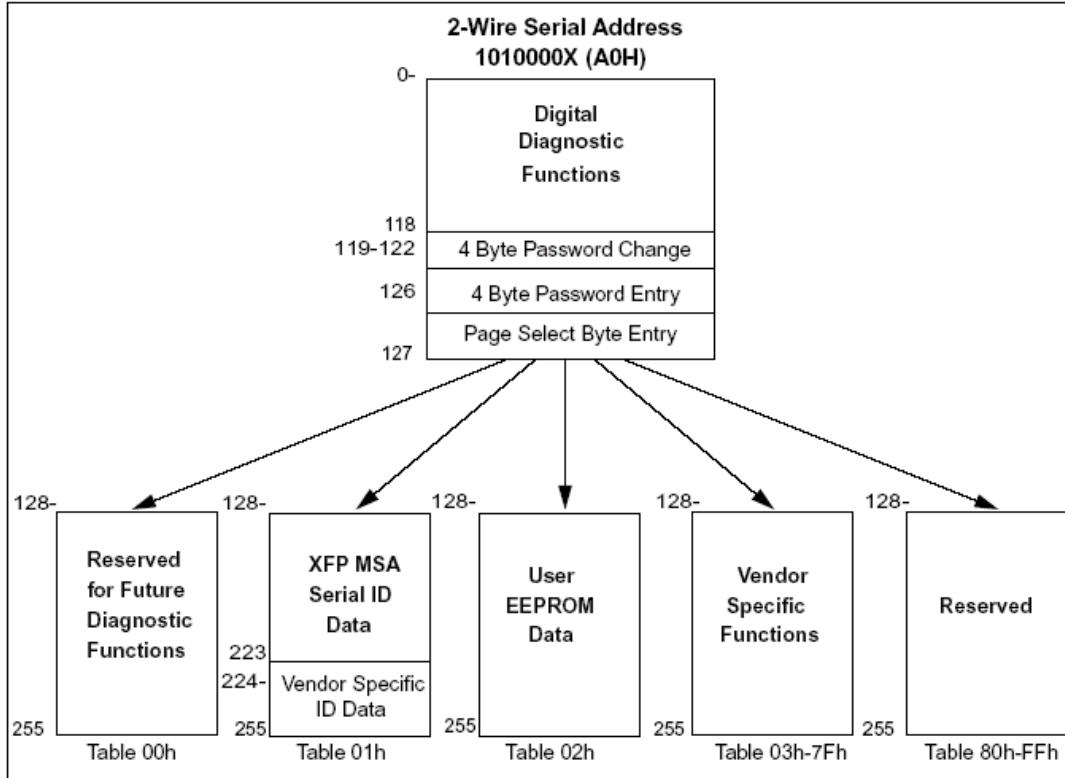


Figure 1. 2-wire Serial Digital Diagnostic Memory Map

Table 1 Monitoring Specification

Data Address	Parameter	Accuracy
96 ~ 97	Temperature	± 3°C
98 ~ 99	Reserved	
100 ~ 101	Tx Bias	± 10%
102 ~ 103	Tx Power	± 2dB
104 ~ 105	Rx Power	± 2dB
106 ~ 107	Vcc3	± 3%

CONNECTION DIAGRAM

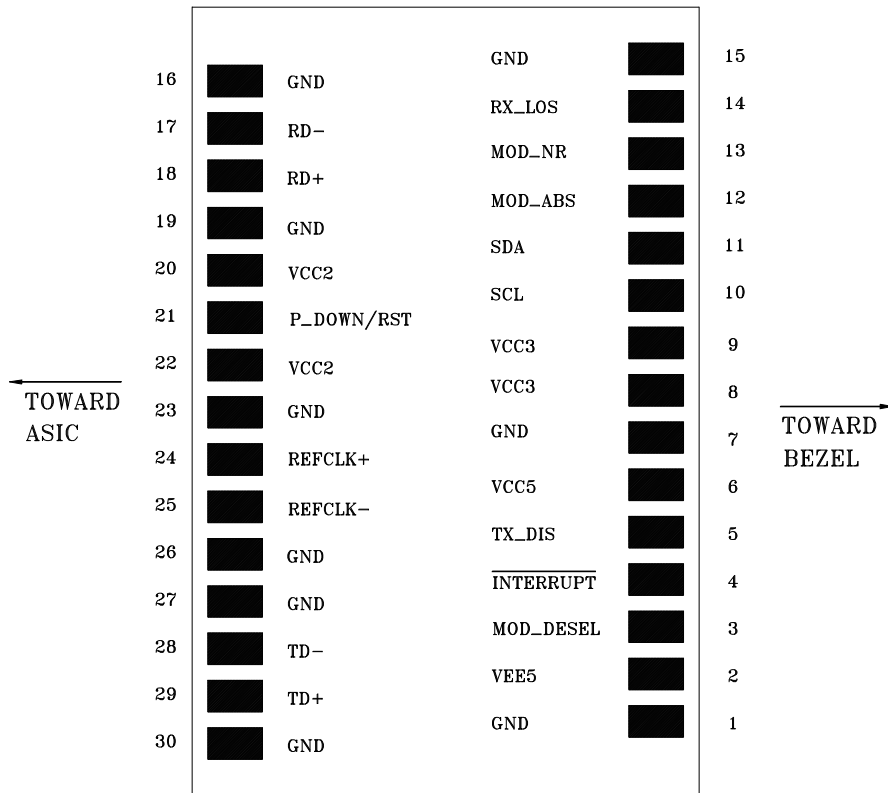


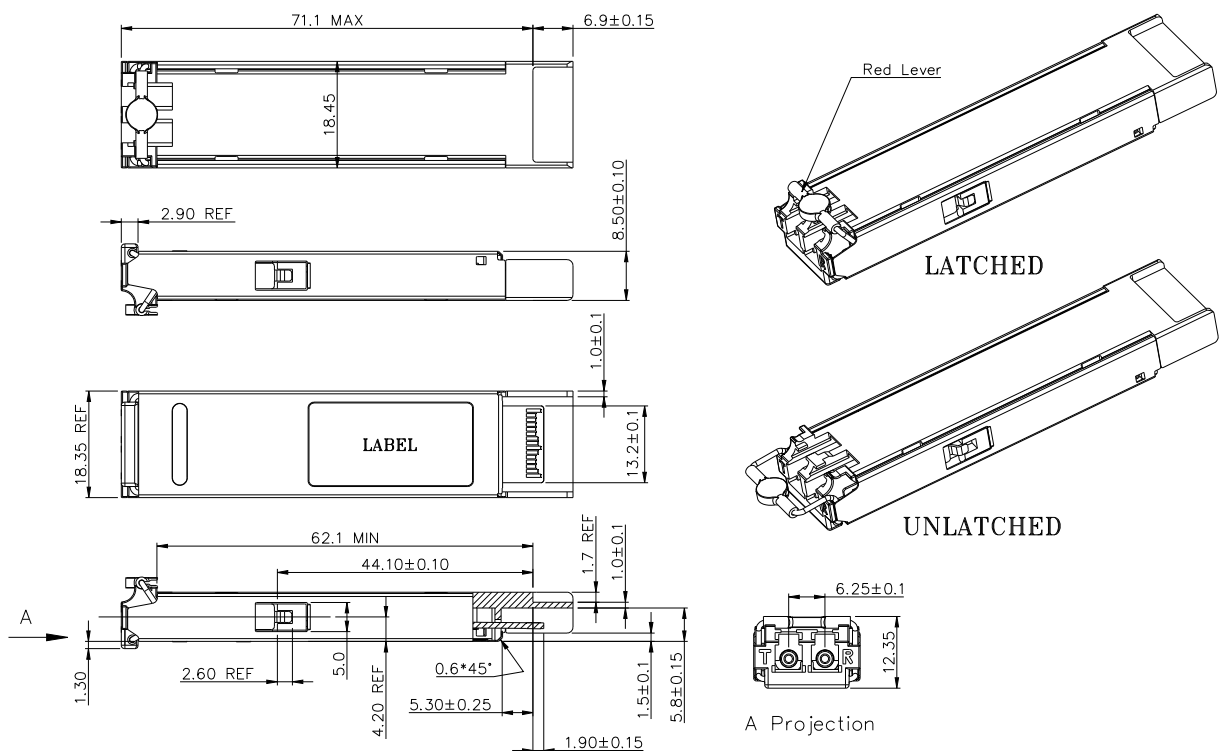
Table 2 PIN Description

PIN	Logic	Signal Name	Description	Note
1		GND	Module Ground	1
2		VEE5	-5.2V Power Supply (Not required)	3
3	LVTTL-I	Mod_Desel	Module De-select; When held low allows module to respond to 2-wire serial interface	
4	LVTTL-O	Interrupt	Interrupt; Indicates presence of an important condition which can be read over the 2-wire serial interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Turns off transmitter laser output	
6		VCC5	+5V Power Supply	3
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I/O	SCL	Serial 2-wire interface clock	2
11	LVTTL-I/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Indicates Module is not present. Grounded in the Module	2
13	LVTTL-O	Mod_NR	Module Not Ready; Indicating Module Operational Fault	2
14	LVTTL-O	RX_LOS	Receiver Loss Of Signal Indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver Inverted Data Output	
18	CML-O	RD+	Receiver Non-Inverted Data Output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply (Not required)	3

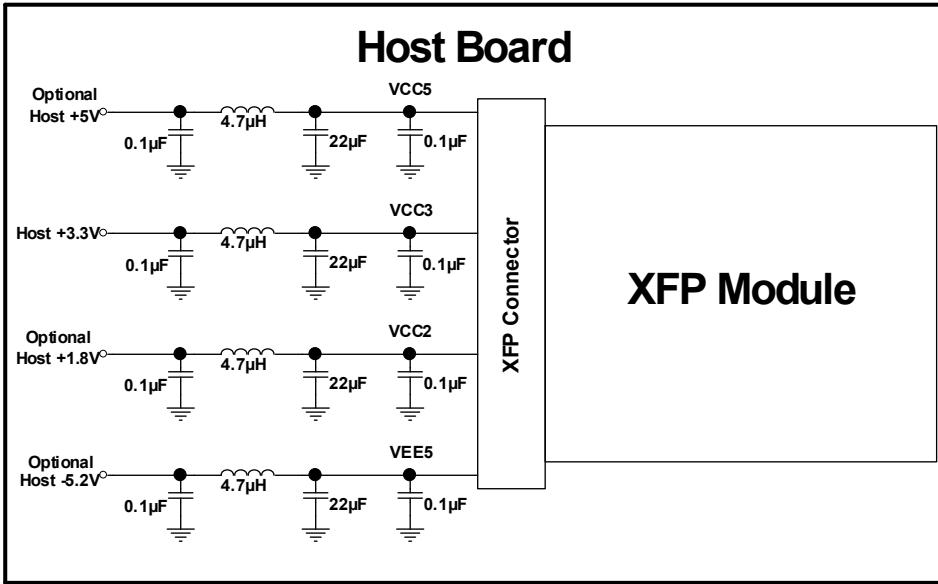
21	LVTTTL-I	P_Down/RST	Power down; When high, requires the module to limit power consumption to 1.5W or below. 2-Wire serial interface must be functional in the low power mode. Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply (Not required)	3
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock Non-Inverted Input, AC coupled on the host board. (Not used. Internally terminated to 50 ohm (100 ohm diff.))	4
25	PECL-I	RefCLK-	Reference Clock Inverted Input, AC coupled on the host board. (Not used. Internally terminated to 50 ohm (100 ohm diff.))	4
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter Inverted Data Input	
29	CML-I	TD+	Transmitter Non-Inverted Data Input	
30		GND	Module Ground	1

1. Module ground pins GND are isolated from the module case and chassis ground within the module.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.
3. These PINs are open within module.
4. A Reference Clock input is not required. If present, it will be ignored.

MECHANICAL SPECIFICATION (UNITS IN MM)



RECOMMENDED POWER CIRCUIT SCHEMATIC



RECOMMENDED INTERFACE CIRCUIT

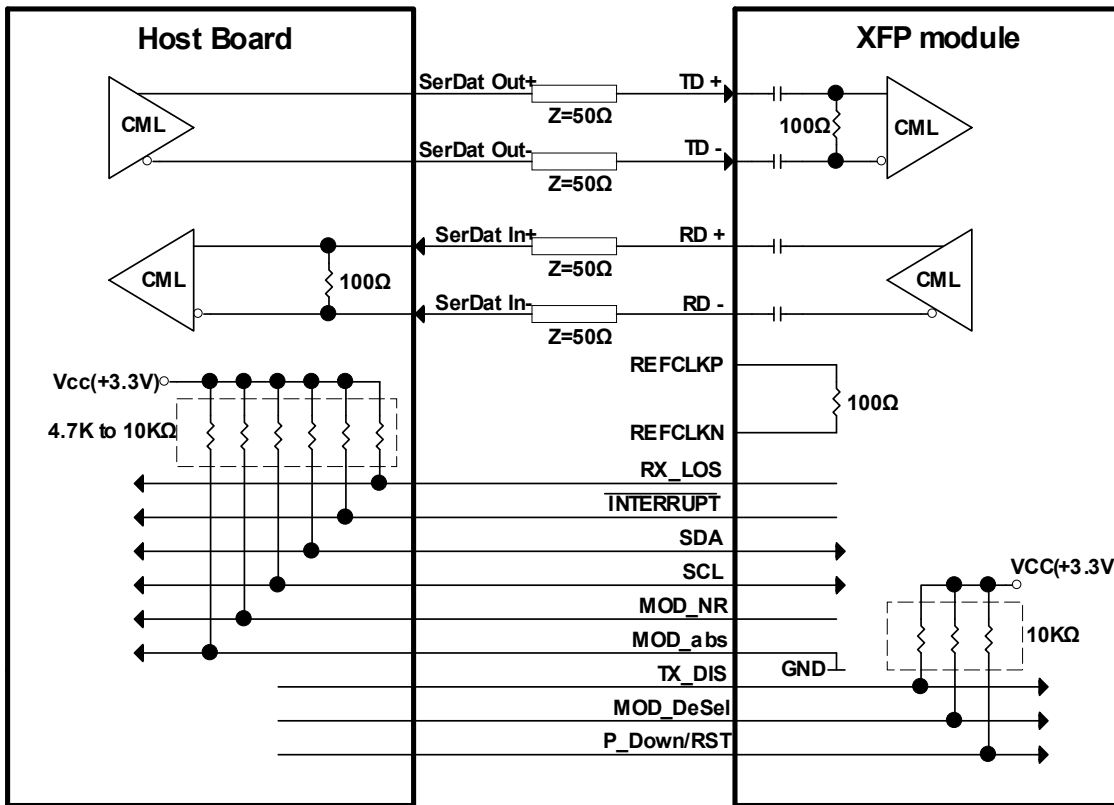


Table 2 Serial ID Memory Contents (Table 01h)

Address	Field Size (Byte)	Name of Filed	Description	Hex
128	1	Identifier	XFP	06
129	1	Ext. Identifier	power consumption < 3.5W, no Ref Clock required	90
130	1	Connector type	LC connector	07
131~138	8	Transceiver	800-SM-LL-L	00 00 00 00 00 00 00 00
139	1	Encoding	8B/10B, NRZ	50
140	1	BR-Min	1.063Gbps	0A
141	1	BR-Max	8.5Gbps	55
142	1	length (SMF)-Km	40 km	28
143	1	Length (E-50μm)	0 m	00
144	1	Length (50 μm)	0 m	00
145	1	Length (62.5 μm)	0 m	00
146	1	Length (Copper)	0 m	00
147	1	Device Tech	DWDM EML, PIN detector	74
148~163	16	Vendor name	OPTOWAY	4F 50 54 4F 57 41 59 20 20 20 20 20 20 20 20 20
164	1	CDR Support	CDR supports 8.5G ~ 1.063G, XFI Loopback	01
165~167	3	Vendor OUI		00 0E FA
168~183	16	Vendor PN	XPS-4341W-DXXG	58 50 53 2D 34 33 34 31 57 2D 44 3x 3x 47 20 20
184~185	2	Vendor rev	ASCII ("31 61" means 1a revision)	xx xx
186~187	2	Wavelength	1XXX.XXnm	xx xx
188~189	2	Wavelength Tolerance	+/- 0.1nm	00 14
190	1	Max Case Temp	70deg	46
191	1	CC_BASE	Check sum of Byte 128 -- 190	
192~195	4	Power Supply	3.5 Wmax, 1.5W pd_max , 750mA 3.3V, 500 mA 5V	AF 96 A8 00
196~211	16	Vendor SN	ASCII	xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx
212~219	8	Date code	ASCII Year (2 Byte), Month (2 Byte), Day (2 Byte)	xx xx xx xx xx xx 20 20
220	1	Diagnostic Monitoring Type	No BER Support, Average Power	08
221	1	Enhanced Options	Optional Soft TX_DISABLE implemented, Optional Soft P_down implemented	60
222	1	Aux Monitoring	AUX1 for Vcc3, AUX2 for Vcc5.	76
223	1	CC_EXT	Check sum of Byte 192 -- 222	
224~255	32	Vendor Specific		Reserved

Note: Specifications subject to change without notice.

REVISION HISTORY

Version	Subject	Release Date
1.0	Initial datasheet	2010/7/1
2.0	Add 100GHz ITU Grid Channel # 19, 20 and 61	2016/1/5
3.0	Revise package diagram	2017/10/12