SPS-2110VW-1T1RG / SPS-2110BVW-1T1RG / SPS-2110AVW-1T1RG (RoHS Compliant)

12 Gb/s / 1310 nm Medium Power Optical SM Digital Diagnostic SFP+ Transmitter/Receiver

FEATURES

- SMPTE 2082, SMPTE 424M, SMPTE 292M, SMPTE 259M, and DVB-ASI Compatible
- Hot-Pluggable SFP Footprint LC Optical Transceiver
- Speed up to 12 Gb/s
- Distance up to 10 km for 12G-SDI
- Reclocker built-in
- Support Video Pathological Patterns for HD-SDI, 3G-SDI, 6G-SDI, and 12G-SDI
- Single Transmitter with Simplex LC
- Single Receiver with Simplex LC
- Based on Industry Standard SFP +
- SFF-8472 Digital Diagnostic Function
- Single +3.3 V Power Supply
- RoHS Compliant
- 0 to 70ºC Operation: SPS-2110VW-1T1RG
- -10 to 85ºC Operation: SPS-2110BVW-1T1RG
- -40 to 85ºC Operation: SPS-2110AVW-1T1RG
- Class 1 Laser International Safety Standard IEC-60825 Compliant

APPLICATIONS

- SMPTE 2082 Compliant Electrical-to-Optical Interfaces
- High-density Video Routers

DESCRIPTION

The SPS-2110VW-1T1RG series is a single mode transceiver module designed to transmit/receive optical serial digital signals as defined in SMPTE 2082, SMPTE 424M, SMPTE 292M, SMPTE 259M, and DVB-ASI. It supports up to 12Gbps and is specifically designed to transmit the pathological patterns for HD-SDI, 3G-SDI, 6G-SDI, and 12G-SDI. It is with the SFP+ 20-pin connector to allow hot plug capability. Digital diagnostic functions are available via an I^2C. The transmitter section uses a 1310 nm multiple quantum well DFB laser and is a class 1 laser compliant according to International Safety Standard IEC-60825. The receiver section uses an integrated InGaAs detector preamplifier (IDP) mounted in an optical header and a limiting post-amplifier IC. A maximum distance of 10 km is achievable with 12Gbps pathological signals.

LASER SAFETY

This single mode transceiver is a Class 1 laser product. It complies with IEC-60825 and FDA 21 CFR 1040.10 and 1040.11. The transceiver must be operated within the specified temperature and voltage limits. The optical ports of the module shall be terminated with an optical connector or with a dust plug.

ORDER INFORMATION

P/No.	Type	Bit Rate (Gb/s)	TX		RX		Package	Temp (ºC)	RoHS Compliant
			λ (nm)	Power (dBm)	λ (nm)	Sen. (dBm)			
SPS-2110VW-1T1RG	Transceiver	Up to 12	1310 DFB	1 to -5	1260/1620	-2 to -13	LC SFP+ with DMI	0 to 70	Yes
SPS-2110BVW-1T1RG	Transceiver	Up to 12	1310 DFB	1 to -5	1260/1620	-2 to -13	LC SFP+ with DMI	-10 to 85	Yes
SPS-2110AVW-1T1RG	Transceiver	Up to 12	1310 DFB	1 to -5	1260/1620	-2 to -13	LC SFP+ with DMI	-40 to 85	Yes

Absolute Maximum Ratings					
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Notes**
Storage Temperature	Tstg	-40	85	ºC	
Operating Case Temperature	Topr	0	70	ºC	SPS-2110VW-1T1RG
		-10	85		SPS-2110BVW-1T1RG
		-40	85		SPS-2110AVW-1T1RG
Power Supply Voltage	Vcc	-0.5	3.6	V	

Recommended Operating Conditions					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units / Notes**
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case Temperature	Topr	0 -10 -40		70 85 85	°C / SPS-2110VW-1T1RG °C / SPS-2110BVW-1T1RG °C / SPS-2110AVW-1T1RG
Power Supply Current	$I_{CC\ (TX+RX)}$		500	550	mA
Data Rate			11.88		Gb/s

Transmitter Optical Specifications (0°C < Topr < 70°C, 3.13V < Vcc < 3.47V)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Average Launch Power	$Po_{,\ Avg}$	-5		1	dBm	1
Output Center Wavelength	λc	1260	1310	1360	nm	
Output Spectrum Width	σλ			1	nm	-20 dB width
Side Mode Suppression Ratio	SMSR	30			dB	
Extinction Ratio	ER	3.5				
Relative Intensity Noise	RIN			-128	dB/Hz	
Average Launch Power of OFF Transmitter				-30	dBm	

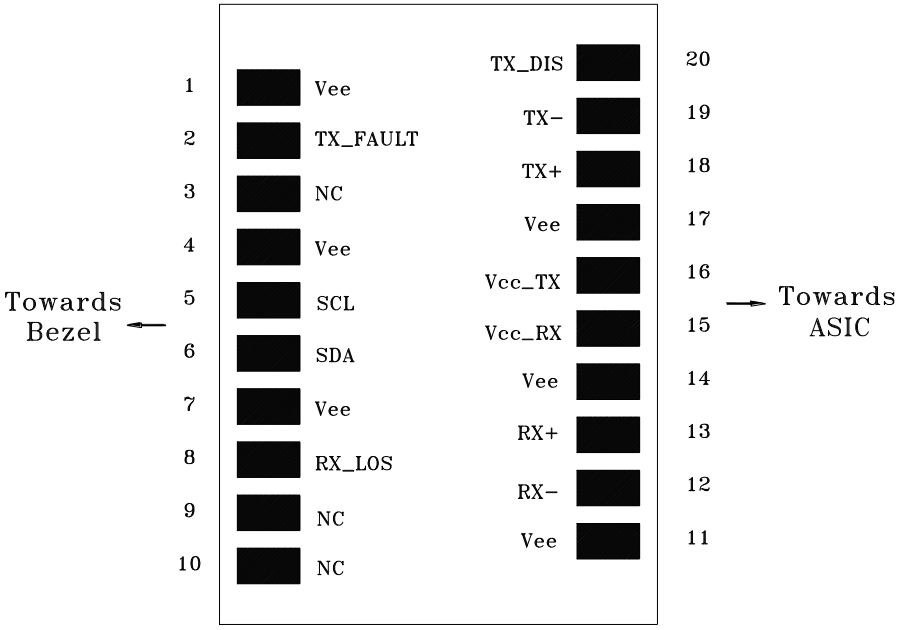
1. Output power is power coupled into a 9/125 μm single-mode fiber.

Receiver Optical Specifications (0°C < Topr < 70°C, 3.13V < Vcc < 3.47V)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Sensitivity@11.88Gb/s	Sen			-13	dBm	2
Sensitivity@6Gb/s	Sen			-14	dBm	2
Sensitivity@2.97Gb/s	Sen			-14	dBm	2
Sensitivity@1.485Gb/s	Sen			-14	dBm	2
Receiver Overload	P_{MAX}	-2	---		dBm	
LOS -- Deasserted	LOS_D	---	---	-14	dBm	Transition: low to high
LOS -- Asserted	LOS_A	-30	---	---	dBm	Transition: high to low
LOS Hysteresis	Hys	0.5	2		dB	
Wavelength of Operation	λc	1260		1620	nm	

2. Measured with pathological pattern @ 1310nm; BER < 10^{-12} .

Electrical Characteristics						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
High-Speed Signal (CML) Interface Specification						
Input Data Rate			11.88		Gb/s	
Differential Input Impedance	Rin		100		Ω	
Output Data Rate			11.88		Gb/s	
Differential Output Impedance	Rout		100		Ω	
Low-Speed Signal (LVTTL) Interface Specification						
Input High Voltage		2.0		Vcc+0.3	V	
Input Low Voltage		GND		0.8	V	
Output High Voltage		2.4		Vcc	V	
Output Low Voltage		GND		0.5	V	

CONNECTION DIAGRAM



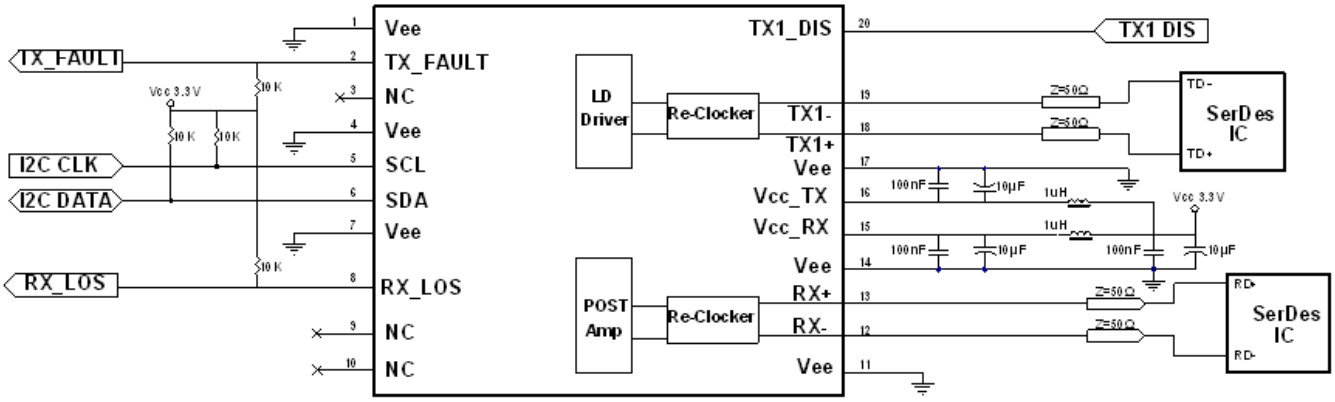
PIN	Name	Function	Notes
1	Vee	Signal Ground	
2	NC	No Connection	
3	NC	No Connection	
4	Vee	Signal Ground	
5	SCL	Serial I^2C Clock	
6	SDA	Serial I^2C Data	
7	Vee	Signal Ground	
8	NC	No Connection	
9	NC	No Connection	
10	NC	No Connection	
11	Vee	Signal Ground	
12	RX-	Negative Differential Output	AC coupled differential lines with 100 ohm differential termination inside the module
13	RX+	Positive Differential Output	
14	Vee	Signal Ground	
15	Vcc RX	Power Supply	+3.3V±5%, Internal connected
16	Vcc TX	Power Supply	
17	Vee	Signal Ground	
18	TX+	Positive Transmitter Data In	AC coupled differential lines with 100 ohm differential termination inside the module
19	TX-	Negative Transmitter Data In	
20	TX_DIS	Transmitter Disable	Internal 4.7 kΩ pull-up. The bias current and modulation current are turned off if TX1_DIS = HIGH.

MODULE DEFINITION

Module Definition	PIN 5	PIN 6	Interpretation by Host
4	SCL	SDA	Serial module definition protocol

Module Definition 4 specifies a serial definition protocol. For this definition, upon power up, SCL and SDA appear as no connector (NC). When the host system detects this condition, it activates the serial protocol. The protocol uses the 2-wire serial CMOS E^2PROM protocol of the ATMEL AT24C01A/02/04 family of components.

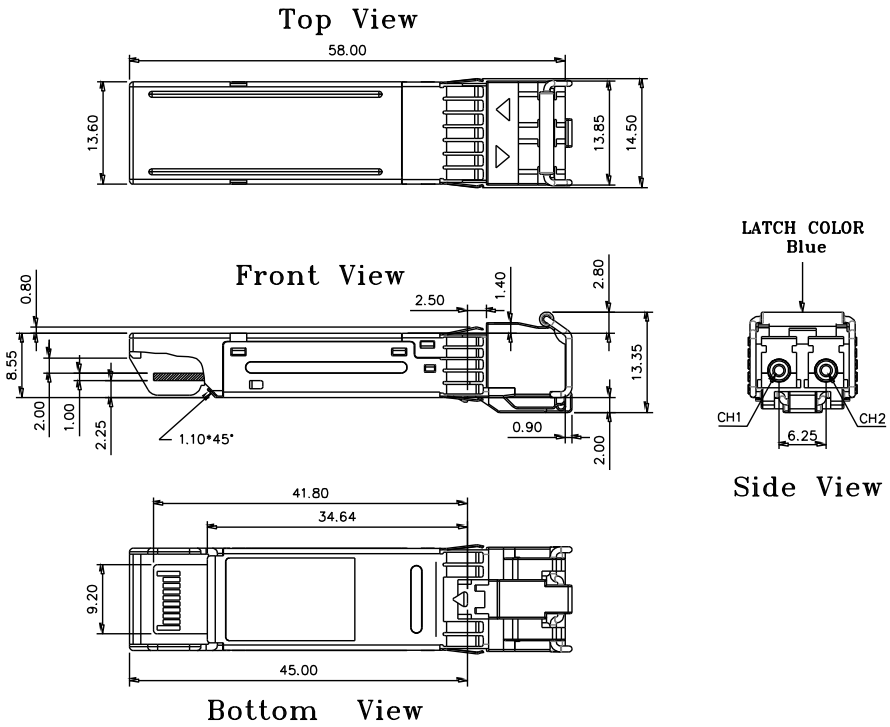
RECOMMENDED CIRCUIT SCHEMATIC



1. Consult the Chipset manufacturer's applications information for biasing required for TX outputs. Some chipset outputs are internally biased and may not need external bias resistor.

PACKAGE DIAGRAM

Units in mm



Note: Specifications subject to change without notice.

REVISION HISTORY

Version	Subject	Release Date
1.0	Initial datasheet	2017/5/19
2.0	1. Add “Reclocker built-in”. 2. Revise power supply current 3. Revise recommended circuit schematic 4. Revise package diagram	2017/11/23
2.1	Remove typo error of FEATURES: SFP MSA compatible	2018/4/30
3.0	Update sensitivity specification as -13dBm @ 12G and -14dBm @ 6G/3G/1.5G	2019/1/25
4.0	Update Recommended circuit schematic	2019/8/12
5.0	Add SPS-2112BVW-1T1RG , SPS-2112AVW-1T1RG	2022/12/1